## REMARKS

Claims 1-21 are all the claims pending in the application. Claims 1-21 stand rejected on prior art grounds. Applicant respectfully traverse these objections/rejections based on the following discussion.

### I. The Prior Art Rejections

Claims 1-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Aguilar, et al. (U.S. Pat. No. 6,199,137) in view of Clark, et al., hereinafter "Clark" (5,425,022). Applicant respectfully traverses this rejection because the prior art of record does not teach or suggest selectively engaging different numbers of serial lanes to alter the speed of data passing through a core.

The Office Action admits that Aguilar does not disclose selectively engaging serial lanes to alter speed of data passing through the core. The Office Action refers to Clark as teaching such a feature. However, Applicant respectfully submits that Clark only discloses a distributed multiplexer that is made up of a number of switches and is utilized in a daisy chain configuration to convert high-speed, time-division multiplex data streams into non-multiplex low-speed data streams to allow high-speed and low-speed data channels to interact (column 3, line 59-column 4, line 4). Clark does not teach or suggest any situation or structure where different numbers of serial lanes can be selectively engaged to alter the speed of data passing through the core as defined by independent claims 1, 8, and 15 where they define that the "selector selectively engages different numbers of said serial lanes to alter a speed of data passing through said core."

Clark teaches some of the fundamentals of the claimed parallel serial architecture that were being developed in the early 1990s and is a structure that the invention and Aguilar have built upon. For example, in column 1, lines 14-20, Clark describes that is necessary to use a multiplexer to switch between low-speed data channels and high-speed data channels. However, Clark notes that the multiplexers available in the early 1990s were incapable of performing

Clark notes that the multiplexers available in the early 1990s were incapable of performing efficient multiplexing operations (column 1, lines 33-41). Therefore, as described in column 2; lines 24-26, Clark states that its improved multiplexer will perform switching functions in parallel rather than serially, which will make the multiplexer much more efficient. In essence, then, Clark is describing some of the fundamental of the parallel serial architecture upon which the present invention and the invention in Aguilar were built.

The claim language requires that the selector (multiplexer) selectively engage different numbers of serial lanes so as to alter the speed of data passing through the core. To the contrary, Clark always utilizes the same number of serial lanes and the same number of buffers and does not increase or decrease the number of serial lanes or buffers engaged so as to alter the speed of data passing through the core. For example, as shown in Figure 1 of Clark, the aggregate switch modules (A1-Am) receive and transmit high-speed time-division multiplex data streams and, through the operation of the lookup table control module 2, de-multiplex this information down to the non-multiplex port switches (P1-Pn) as discussed in greater detail in column 3, line 59-column 4, line 29. Therefore, Clark consistently utilizes the same number of serial lanes and the same number of buffers throughout all processing environments, and there is no structure within Clark whereby certain serial lanes can be selectively used or not used.

Therefore, it is Applicant's position that Clark does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. As shown in Applicant' Figure 2B, the multiplexers 215, 236 selectively engage a different number of data lanes 225 (e.g., alter the lane width) in order to perform a speed reduction between the transmission media 280 and the ASIC 246. For example, with the exemplary structure shown in FIG. 2B, the invention can perform speed reduction by simultaneously transmitting the data along four lanes.

To illustrate the utility of the invention, given that 12 data lanes are used in a network, when in a 4X reduction mode of operation, physical data lanes 4-11 can be used as wider extensions of lanes 0-3. Further, when in a 1X mode of operation using these 12 data lanes,

FIFOs for data lanes 1-11 can be a wider extension of the FIFO used for data lane 0, thereby achieving up to a 12X speed reduction. Thus, when data is accessed at the transmission media 280, by using the multiplexers 215, 236, the upper link layer 250 can access wider data at a slower rate. The invention also produces an advantage in that receive elastic FIFO buffers 220 perform the function of the frequency correction portion 260 and correct any frequency deviations which may occur along the transmission media 280. FIFO buffers 220, 230 also modify the frequency of the signal to that desired by the ASIC 246. Therefore, the FIFO buffers 220 perform the functions that were previously performed by FIFO buffers 251 and 261 shown in FIG. 2A, thereby reducing the number of buffers within the core logic 210. This decrease in the number of buffers within the core logic 210 reduces power consumption, increases processing speed and decreases the chip area consumed by the core logic 210.

Thus, as mentioned above, Aguilar does not teach selectively engaging serial lanes to alter the data speed and Clark also does not teach this feature. Therefore, the proposed combination of Aguilar and Clark does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. Therefore, it is Applicant's position that the proposed combination of Aguilar and Clark does not render obvious independent claims 1, 8, and 15 and that such claims are patentable over the prior art of record. Further, dependent claims 2-7, 9-14, and 16-21 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

## II. Formal Matters and Conclusion

In view of the foregoing, Applicant submits that claims 1-21, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at

the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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